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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/726,561	12/04/2003	Kazunari Aoyama	392.1846	5449

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EXAMINER	
ALPHONSE, FRITZ	
ART UNIT	**PAPER NUMBER**
2112	
MAIL DATE	**DELIVERY MODE**
10/15/2007	PAPER

Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Office Action Summary	Application No.	Applicant(s)	
	10/726,561	AOYAMA ET AL.	
	Examiner	Art Unit	
	Fritz Alphonse	2112	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *24 July 2007*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-9 and 13* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-5,7-9 and 13* is/are rejected.

7)☒ Claim(s) *6* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *04 December 2003* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

0.1 This Office Action is in response to the Request for Continuation Examination (RCE) filed on 7/24/2007. Claims 10-12 are canceled; claim 13 is added.

Continued Examination Under 37 CFR 1.114

1. A request for continued examination under 37 CFR 1.114; including the fee set forth in 37 CFR 1.17(e), was filed in this application after final rejection. Since this application is eligible for continued examination under 37 CFR 1.114, and the fee set forth in 37 CFR 1.17(e) has been timely paid, the finality of the previous Office action has been withdrawn pursuant to 37 CFR 1.114. Applicant's submission filed on 2/20/2007 has been entered.

Claim Rejections - 35 USC § 103

2. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

3. Claims 1-5, 7-9 and 13 are rejected under 35 U.S.C. 103(a) as being unpatentable over Zulian (U.S. Pat. No. 5,701,413) in view of Byers (U.S. Pat. No. 5,535,405) in view of Watanabe (U.S. Pat. No. 5,260,951)

As to claim 1, Zulian (fig. 1) shows an error detection/correction system in data transmission between a plurality of modules (i.e., stations 1-8), the system including a plurality of error detection/correction code generation circuits having a difference in at least one of an inspection bit length, an information bit length, and a correction capacity (col. 4, lines 16-48),

and error detection/correction circuits corresponding to the error detection/correction code generation circuits are built into the system (col. 13, lines 43-47).

Zulian does not explicitly disclose a plurality of modules connected via buses in a controller.

However, the limitation is obvious and well known in the art, as evidenced by Byers (fig. 5).

Therefore, it would have been obvious to a person of ordinary skill in the art at the time of the invention to improve upon the multi-processor computer system, as disclosed by Byers. Doing so would efficiently control the operation of special purpose gate arrays intended to store and transfer data between a special purpose gate array and an external device or system and between special purpose gate arrays.

In addition, as to claim 1, Zulian does not explicitly disclose an error detection/correction code generation circuit and error detection/correction circuit are switched over dependent upon a kind, a length, and a timing of the data to be transferred.

However, in the same field of endeavor, Watanabe discloses an error detection circuit for digital data, wherein an error detection/correction code generation circuit and error detection/correction circuit are switched over dependent upon a kind, a length, and a timing of the data to be transferred (col. 1 lines 62 through col. 2 line 14).

Therefore, it would have been obvious to a person of ordinary skill in the art at the time of the invention to combine Zulian with the decoding system, as disclosed by Kikuchi. Doing so would improve an improved system for data communication in which digital data can be properly reconverted (col. 1, lines 58061).

As to claims 2-4, Zulian discloses the limitations as claimed. Zulian does not explicitly disclose an error detection/correction system, wherein the error detection/correction system switches over between error detection/correction codes to be used dependent upon on a phase of transmitting an address, a command, and data; and, wherein the error detection/correction system switches over between error detection/correction codes to be used, dependent upon a data quantity to be transferred.

However, the limitations are disclosed by Watanabe (col. 17, lines 49 through col. 18 line). See the motivation for the same reason disclosed in claim 1 above.

As to claims 5, 7-9, Zulian (fig. 1) does not explicitly disclose a controller in which a plurality of modules that adopt the error detection/correction system are connected via buses.

However, the limitation is obvious and well known in the art, as evidenced by Byers (fig. 5).

Therefore, it would have been obvious to a person of ordinary skill in the art at the time of the invention to improve upon the multi-processor computer system, as disclosed by Byers. Doing so would efficiently control the operation of special purpose gate arrays intended to store and transfer data between a special purpose gate array and an external device or system and between special purpose gate arrays.

As to claim 13, the claim has substantially the limitations of claim 1; therefore, it is analyzed as previously discussed in claim 1 above.

Allowable Subject Matter

4. Claim 6 is objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

Claim 6 contains allowable because none of the cited references either singular or in combination discloses and error correcting coding method including "controller comprises a serial transfer module that connects a plurality buses connected with the plurality of modules, by means of a serial transmission line, and a plurality of error detection/correction code generation circuits having a difference in at least one of an inspection bit length, an information bit length, and a correction capacity, and error detection/correction circuits corresponding to the error detection/correction code generation circuits are built into the serial transfer module, and the error detection/correction system is used also for the serial transfer."

Response to Arguments

5. Applicant's arguments filed on 2/20/2007 have been fully considered but they are not persuasive.

Applicant argues "Zulian does not disclose any of the features as recited in claim 1."

The Examiner respectfully disagrees because Zulian clearly discloses the limitations of the claims: a plurality of modules (i.e., stations 1-8), the system including a plurality of error detection/correction code generation circuits having a difference in at least one of an inspection bit length, an information bit length, and a correction capacity (col. 4, lines 16-48), and error detection/correction circuits corresponding to the error detection/correction code generation circuits are built into the system (col. 13, lines 43-47).

Conclusion

6. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure. See PTO-892.

Any response to this action should be mailed to:

Commissioner of Patents and Trademarks, Washington, D.C. 20231

or faxed to: (703) 872-9306 for all formal communications.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Fritz Alphonse, whose telephone number is (571) 272-3813. The examiner can normally be reached on M-F, 8:30-6:00, Alt. Mondays off.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Jacques Louis-Jacques, can be reached at (571) 272-6962.

Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the Group receptionist whose telephone number is (571) 272-3824

Information regarding the status of an application may also be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Fritz Alphonse

Art Unit 2112

October 9, 2007